Advanced VLSI Design – Elec522

Rice University – Fall 2011, Abercrombie Labs AL A116

The goals of the course are to study design methodologies for application-specific processors for applications particularly in wireless communications. The course includes a design project initially targeted to an FPGA. In some years, chips may be fabricated by MOSIS depending on project topics.

Course Instructors:

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Lab Assistant:

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Homework Assignments

Approximately 5 Assignments on ASIC and FPGA Design using Xilinx System Generator tools, along with Xilinx ISE tools. Also, some assignments may use Xilinx Platform Studio for embedded systems, Transport Triggered Architecture MOVE tools for ASIP Design, and Synopsys DC Ultra for ASIC synthesis. We may also use the Cadence SOC Encounter tools in the ASIC flow for System on Chip integration and Mentor Graphics Catapult-C and Xilinx AutoESL AutoPilot for high level synthesis.

Projects for Fall 2011 and Presentation

Final design project to be implemented on an FPGA, and also targeted to an ASIC library. Possible fabrication through the MOSIS service. A presentation will be given in class on the project, and additional presentations of research papers will be assigned for discussion. Previous year topics have included a systolic array co-processor for matrix factorization and solution of systems of linear equations.

Course Contents

The topics covered in this course include:

- Design methodology for ASIC and FPGA implementations
- FPGA hardware structures and fabrics

- Review of Combinational Logic, Sequential Machines, and Architecture
- High-level VLSI synthesis and design tools including Synopsys, Cadence, Mentor Graphics, with CAD algorithm overview for floorplanning, placement, and routing in ASICs.
- High-level DSP algorithm simulation and code (VHDL) generation using Xilinx System Generator, and possibly Catapult-C, and Synfora PICO.
- Design and analysis of algorithm-specific VLSI processor architectures. Topics include the implementation of pipelined and systolic processor structure. Techniques for mapping numerical algorithms onto custom processor arrays. including Application Specific Instruction Processors (ASIPs).
- High-level Design frameworks for systems containing custom and general-purpose units.
- Prototyping using Xilinx System Generator, Xilinx ISE tools and Xilinx FPGAs.
- Adaptive computing as a technology for reconfigurable wireless systems.
- Example architectures: Blackfin, TigerSHARC, XPP, Sandblaster, TI TCI platform, picoArray.
- Heterogeneous DSP-FPGA-ASIC processors for wireless handsets

Prerequisites

A course in Digital Systems Design such as ELEC 326/327. An introductory course in VLSI System Design is useful. Background in computer architecture, computer arithmetic, and signal processing is also helpful.

Course Materials

- Wayne Wolf, “FPGA-Based System Design,” Prentice Hall, 2004, ISBN 0-13-142461-0 Emphasis on Chapters 1, 3, 6, 7 (about 250 pages). http://www.amazon.com/FPGA-Based-System-Design-Prentice-Semiconductor/dp/0131424610/ref=sr_1_3/102-0171952-4496933?ie=UTF8&s=books&qid=1188319895&sr=1-3
- Walter Tuttlebee, Editor, “Software Defined Radio, Baseband Technology for 3G Handsets and Basestations,” John Wiley and Sons, 2004, ISBN 0-470-86770-1 Emphasis on Chapters 1, 2, 3, 4, 5, 6, 7, 10, 11. (about 250 pages). http://www.amazon.com/Software-Defined-Radio-Technologies-Basestations/dp/0470867701/ref=sr_1_2/102-0171952-4496933?ie=UTF8&s=books&qid=1188320142&sr=1-2

Also current research papers and design tool tutorials to be distributed in class.
Papers (from IEEE Explore) are on ASIP design, and example architectures, (about 100 pages) including:

- From ASIC to ASIP: The Next Design Discontinuity

- Approaches to Low-Power Implementations of DSP Systems
- Custom-Instruction Synthesis for Extensible-Processor Platforms
- Issues and Approaches to Coarse-Grain Reconfigurable Architecture Development
- Design of Transport Triggered Architectures
- Design of Transport Triggered Architecture Processor for Discrete Cosine Transform
- Immediate Optimization for Compressed Transport Triggered Architecture Instructions
- ILP Architectures: Trading Hardware for Software Complexity
- ASIP Architecture Implementation of Channel Equalization Algorithms for MIMO Systems in WCDMA Downlink
- Design Space Exploration for Real-Time Embedded Stream Processors
- Semi-Parallel Reconfigurable Architectures for Real-Time LDPC Decoding
- Rapid Scheduling of Efficient VLSI Architectures for Next-Generation HSDPA Wireless System Using Precision-C Synthesizer

Laboratory Use:

We will use the VLSI Lab, AL A116, in Abercrombie Labs with the Xilinx Virtex II-Pro University Development Board for the course. We will also use the Rice University WARP board containing a Virtex 4 FPGA. We will also use the Rice CLEAR Linux cluster for access to VLSI design tools via Xwindows using Xming in addition to the laboratory PCs in AL A116.

Joe Cavallaro Updated 22 August 2011